DIGITAL TECHNIQUES AND MICROPROCESSORS **Course Code : 313305**

Programme Name/s	**: Cloud Computing and Big Data/ Information Technology/ Computer Science & Information Technology**
Programme Code	**: BD/ IF/ IH**
Semester	**: Third**
Course Title	**: DIGITAL TECHNIQUES AND MICROPROCESSORS**
Course Code	**: 313305**

I. RATIONALE

It is essential to know the basics of digital techniques for understanding the applications of digital systems as well as microprocessors. Microprocessors serve as the heart of computer systems, and understanding their architecture is crucial for appreciating how computers process information. Microprocessors play a key role in embedded systems and Internet of Things (IoT) devices, making this course highly relevant for contemporary applications in IT. This course will help the student to comprehend logic and circuit design and enable them to perform assembly language programming for microprocessors, cultivating the skills essential for logic and software development in the IT sector.

II. INDUSTRY / EMPLOYER EXPECTED OUTCOME

This course aims to help the student to attain the following industry identified outcomes through various teaching-learning experiences:
Test digital systems by applying principles of digital techniques and microprocessors.

III. COURSE LEVEL LEARNING OUTCOMES (COS)

Students will be able to achieve & demonstrate the following COs on completion of course based learning

- CO1 - Test logic gates and digital systems.
- CO2 - Use basic combinational and sequential logic circuits employing digital ICs.
- CO3 - Perform operations on registers using 8086 instructions.
- CO4 - Use 8086 microprocessor environment to build and execute assembly language programs.
- CO5 - Develop assembly language programming in 8086 to implement loops and branching instructions.

IV. TEACHING-LEARNING & ASSESSMENT SCHEME

Course Code	Course Title	Abbr	Course Category/s	Learning Scheme					Credits	Assessment Scheme											
				Actual Contact Hrs./Week			SLH	NLH		Paper Duration	Theory				Based on LL & TL				Based on SL		Total Marks
															Practical						
				CL	TL	LL					FA-TH	SA-TH	Total		FA-PR		SA-PR		SLA		
											Max	Max	Max	Min	Max	Min	Max	Min	Max	Min	
313305	DIGITAL TECHNIQUES AND MICROPROCESSORS	DTM	AEC	3	-	2	1	6	3	3	30	70	100	40	25	10	25@	10	25	10	175

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Total IKS Hrs for Sem. : 0 Hrs
Abbreviations: CL- ClassRoom Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS - Indian Knowledge System, SLA - Self Learning Assessment
Legends: @ Internal Assessment, # External Assessment, *# On Line Examination , @$ Internal Online Examination
Note :

1. FA-TH represents average of two class tests of 30 marks each conducted during the semester.
2. If candidate is not securing minimum passing marks in FA-PR of any course then the candidate shall be declared as "Detained" in that semester.
3. If candidate is not securing minimum passing marks in SLA of any course then the candidate shall be declared as fail and will have to repeat and resubmit SLA work.
4. Notional Learning hours for the semester are (CL+LL+TL+SL)hrs.* 15 Weeks
5. 1 credit is equivalent to 30 Notional hrs.
6. * Self learning hours shall not be reflected in the Time Table.
7. * Self learning includes micro project / assignment / other activities.

V. THEORY LEARNING OUTCOMES AND ALIGNED COURSE CONTENT

Sr.No	Theory Learning Outcomes (TLO's)aligned to CO's.	Learning content mapped with Theory Learning Outcomes (TLO's) and CO's.	Suggested Learning Pedagogies.
1	TLO 1.1 Convert the given number system to the specified number system. TLO 1.2 Convert given form of code to another code. TLO 1.3 Apply arithmetic operations on the number belongs to given number system. TLO 1.4 Derive the truth table of the given basic logic gates / derived logic gates. TLO 1.5 Design the logical circuit for the given application.	**Unit - I Number Systems and Digital Logic Gates** 1.1 Terms - Bit, Byte, Nibble, Word 1.2 Number systems- Decimal, Binary, Octal, Hexadecimal and their conversions from one number system to another 1.3 Codes and code conversion: BCD, GRAY, ASCII, EBCDIC 1.4 Binary, Hexadecimal, BCD arithmetic and 1's and 2's complement (up to 8 bit) 1.5 Basic logic gates(AND,OR,NOT), universal gates (NAND,NOR), special gates (EX-OR, EX-NOR), and their truth table, basic gates using universal gates 1.6 Basic logic operations using laws of Boolean algebra, De-Morgan's theorems	Classroom Learning Flipped Classroom Collaborative Learning Use of logic simulator like Virtual Labs, online converters etc
2	TLO 2.1 Explain concept of Sum-of- Product (SOP) and Product-of-Sum(POS). TLO 2.2 Explain concept of half-full adder / half-full subtractor using K-MAP. TLO 2.3 Construct the logical diagrams using multiplexer / demultiplexer ICs to solve the given expression. TLO 2.4 State the use of latch, flipflop, counter, buffer.	**Unit - II Combinational and Sequential Logic Circuits** 2.1 Standard/canonical forms for Boolean functions, Min-terms and Max-terms, Minimization of expression using SOP-POS and K-MAP, simplification of expression of half adder/full adder and half/full subtractor using K-MAPs 2.2 Concept of multiplexer and demultiplexer, logical diagram development using multiplexer/ demultiplexer ICs 2.3 Multiplexer tree and demultiplexer tree, applications of multiplexers and demultiplexers 2.4 Clock signal, flipflop, latches, counter, buffer and tri-state buffer (only concept)	Lecture Using Chalk-Board Flipped Classroom Collaborative Learning Virtual Lab

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Sr.No	Theory Learning Outcomes (TLO's)aligned to CO's.	Learning content mapped with Theory Learning Outcomes (TLO's) and CO's.	Suggested Learning Pedagogies.
3	TLO 3.1 Enlist features of 8086 microprocessor. TLO 3.2 Calculate physical address to locate the given data from memory segmentation. TLO 3.3 Explain given blocks of architecture of 8086 microprocessor. TLO 3.4 Compare minimum mode and maximum mode of 8086 features.	**Unit - III 16-Bit Microprocessor 8086** 3.1 Microprocessor 8086 features, pin diagram description and architecture of 8086 3.2 Units of 8086: Bus interface unit and execution unit, concept of memory segmentation and pipelining, physical address generation 3.3 Flag register of 8086, segment registers, index register, ALU-arithmetic logic unit 3.4 Minimum mode and maximum mode configuration of 8086, timing diagrams concept	Classroom Learning Flipped Classroom Cooperative Learning
4	TLO 4.1 Identify relevant addressing mode of instruction. TLO 4.2 Choose relevant instruction to perform the given operation from the instruction set of 8086. TLO 4.3 Use data transfer and arithmetic instruction for given situation employing specific addressing mode. TLO 4.4 Use logical and flag manipulation instruction for given situation employing specific addressing mode.	**Unit - IV Basic assembly Language Programming using 8086** 4.1 Programming model of 8086 assembly language program assembler directives 4.2 Addressing modes of 8086, register, direct, based, indexed, based-indexed addressing, assembler directives 4.3 Format of instruction, instruction set: data transfer, arithmetic, logical, branch and loop, flag manipulation 4.4 Shift and rotate instructions, string instructions	Classroom Learning Collaborative Learning Flipped Classroom Program development tools and simulators
5	TLO 5.1 Develop the assembly language program to solve the given problem using looping. TLO 5.2 Develop the assembly language program to solve the given problem using branching structure.	**Unit - V Assembly Language Programming using Loops and Branching instructions** 5.1 Assembly language programs for addition, subtraction, multiplication, division on hexadecimal, BCD numbers (8/16 bit) 5.2 Assembly language programs using decision making 5.3 Assembly language programs using looping and branching structure. assembly language programs for sorting, searching and block transfer (with string and without string instructions) of given numbers 5.4 Assembly language programs for uppercase to lowercase, lowercase to uppercase, conversion of hexadecimal to BCD and BCD to hexadecimal	Classroom Learning Flipped Classroom Collaborative Learning Program development tools and simulators

VI. LABORATORY LEARNING OUTCOME AND ALIGNED PRACTICAL / TUTORIAL EXPERIENCES.

Practical / Tutorial / Laboratory Learning Outcome (LLO)	Sr No	Laboratory Experiment / Practical Titles / Tutorial Titles	Number of hrs.	Relevant COs

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Practical / Tutorial / Laboratory Learning Outcome (LLO)	Sr No	Laboratory Experiment / Practical Titles / Tutorial Titles	Number of hrs.	Relevant COs
LLO 1.1 Identify various logic gate ICs. LLO 1.2 Verify truth tables of basic logic gates (AND-7408, OR- 7432, NOT-7404) using breadboard LLO 1.3 Verify truth tables of universal gates (NAND-7400, NOR-7402). LLO 1.4 Verify truth tables of special logic gates EX-OR-7486, EX-NOR-74266	1	* Verification of truth table of basic logic gates, special logic gates and Identify various Logic gate ICs.	2	CO1
LLO 2.1 Design a circuit for a given logical expression using the universal gates (NAND) LLO 2.2 Design a circuit for a given logical expression using the universal gates (NOR).	2	Implementation and verification of expression using universal logic gate ICs	2	CO1
LLO 3.1 Verify the truth table of De-Morgan's first theorem using basic logic gates. LLO 3.2 Verify the truth table of De-Morgan's second theorem using basic logic gates..	3	Verification of De-Morgan's theorems using basic logic gates	2	CO2
LLO 4.1 Design and test the circuit for converting expression into Sum-of-Product(SOP) LLO 4.2 Design and test the circuit for converting expression into product (POS).	4	* Conversion of expression to Sum-of-Product (SOP) and Product-of-Sum (POS)	2	CO2
LLO 5.1 Design a Combinational Circuit using Multiplexer IC-74LS153 (4:1 MUX). LLO 5.2 Design a Combinational Circuit using Demultiplexer IC -74139.	5	* Implement Multiplexer and Demultiplexer logic (The practical may be performed using virtual lab)	2	CO2
LLO 6.1 Verify states of the Latch using IC 74373.	6	Implementation of Latch	2	CO2
LLO 7.1 Develop an assembly language program to verify the contents of general purpose, segment registers, flags and contents of memory locations of segments	7	* Verification of contents of general purpose, segment registers, flags and memory locations of different segments during execution of the program	2	CO3
LLO 8.1 Develop an assembly language program to add 8 bit and 16-bit signed/ unsigned hexadecimal numbers. LLO 8.2 Develop an assembly language program to Subtract two 8-bit and 16-bit signed/ unsigned hexadecimal numbers.	8	* Assembly language programming for addition and subtraction for hexadecimal numbers	2	CO4
LLO 9.1 Develop an assembly language program to add 8 bit and 16-bit BCD numbers. LLO 9.2 Develop an assembly language program to subtract two 8-bit and 16-bit BCD numbers.	9	Apply assembly language programming logic for addition, subtraction and multiplication for BCD numbers.	2	CO4
LLO 10.1 Develop assembly language programming for multiplication and division.	10	* Assembly language programming for multiplication and division	2	CO4

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Practical / Tutorial / Laboratory Learning Outcome (LLO)	Sr No	Laboratory Experiment / Practical Titles / Tutorial Titles	Number of hrs.	Relevant COs
LLO 11.1 Develop assembly language programming for finding smallest /largest hexadecimal numbers.	11	Assembly language programming to find smallest /largest hexadecimal numbers	2	CO4
LLO 12.1 Develop an assembly language program to Sort numbers of given arrays in ascending order. LLO 12.2 Develop an assembly language program to Sort numbers of a given array in descending order.	12	* Assembly language programming for sorting of data	2	CO5
LLO 13.1 Develop assembly language programming for transfer of block of data.	13	Assembly language programming for transfer of block of data	2	CO5
LLO 14.1 Apply assembly language programming logic for counting the occurrence of a given number.	14	Count the occurrence of a given number from a block of data	2	CO5
LLO 15.1 Develop an assembly language program to shift given hex number to the left / right(with and without carry). LLO 15.2 Develop an assembly language program to rotate given hex number to the left / right(with and without carry).	15	* Implement shift and rotate instructions on given data	2	CO5

Note : Out of above suggestive LLOs -

- '*' Marked Practicals (LLOs) Are mandatory.
- Minimum 80% of above list of lab experiment are to be performed.
- Judicial mix of LLOs are to be performed to achieve desired outcomes.

VII. SUGGESTED MICRO PROJECT / ASSIGNMENT/ ACTIVITIES FOR SPECIFIC LEARNING / SKILLS DEVELOPMENT (SELF LEARNING)

Micro project

- Find the factorial of a given number using 8086 assembly language programming.
- Separate odd and even numbers from a given array using an assembly language program.
- Design shift register using JK Flipflop.
- Design a Burglar alarm using electronic components and digital ICs.

Assignment

- Write an assembly language program using 8086 to generate the Fibonacci series.
- Draw and implement the circuit on the breadboard for 1:16 DEMUX using 1:8 DEMUX. State the ICs used along with their description.

Self Learning Activity

- Develop an assembly language program to add 8-bit and 16-bit Unsigned numbers (using procedure).
- Write an assembly language program to add and subtract two BCD numbers(using MACRO).
- Write an ALP to multiply two BCD numbers (using MACRO).

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Note :

- Above is just a suggestive list of microprojects and assignments; faculty must prepare their own bank of microprojects, assignments, and activities in a similar way.
- The faculty must allocate judicial mix of tasks, considering the weaknesses and / strengths of the student in acquiring the desired skills.
- If a microproject is assigned, it is expected to be completed as a group activity.
- SLA marks shall be awarded as per the continuous assessment record.
- If the course does not have associated SLA component, above suggestive listings is applicable to Tutorials and maybe considered for FA-PR evaluations.

VIII. LABORATORY EQUIPMENT / INSTRUMENTS / TOOLS / SOFTWARE REQUIRED

Sr.No	Equipment Name with Broad Specifications	Relevant LLO Number
1	1) Digital Multimeter: 3 and 1/2 digit 2) Pulse Generator/Function Generator: TTL Pulse Generator 20mA per Channel(max), 0 to 5.0 V (max) 3) DC Regulated Power Supply: 2 x 0-30 V; 0-2 A Automatic Overload (Current Protection) Constant Voltage and Constant Current Operation Digital Display for Voltage and Current Adjustable Current Limiter Excellent Line and Load Regulation 4) Basic logic gates (AND-7408, OR- 7432, NOT- 7404), Universal gates (NAND-7400, NOR-7402) EX-OR-7486, EX-NOR-74266 5) 4:1 Multiplexer IC-74LS153 6) Demultiplexer IC -74139 7) Bread boards, connecting wires, Stripper, Soldering Gun, Soldering Metal, Flux, IC Tester, LEDs, Digital ICs, Data sheets of ICs used in Lab.	1,2,3,4,5,6
2	1) Personal Computer Intel Pentium Onwards Minimum 2GB RAM. 500Gbyte HDD) installed with Windows 2000 onwards 2) Any Editor to write/edit programs 3) Turbo/Macro Assembler (TASM / MASM) 4) Turbo Linker (TLINK/LINK 5) Turbo Debugger (ID/Debug), (DOSBOX utility for higher-end operating systems) (Minimum 20 computers for a batch of 20 students) with the shared printer. 8086 freeware/open source based simulator to demonstrate internal functioning of microprocessor (Desirable)	8,10,9,11,13,12,14,15,7

IX. SUGGESTED WEIGHTAGE TO LEARNING EFFORTS & ASSESSMENT PURPOSE (Specification Table)

Sr.No	Unit	Unit Title	Aligned COs	Learning Hours	R-Level	U-Level	A-Level	Total Marks
1	I	Number Systems and Digital Logic Gates	CO1	8	2	4	6	12
2	II	Combinational and Sequential Logic Circuits	CO2	10	2	8	6	16
3	III	16-Bit Microprocessor 8086	CO3	8	2	4	6	12
4	IV	Basic assembly Language Programming using 8086	CO4	10	4	6	6	16
5	V	Assembly Language Programming using Loops and Branching instructions	CO5	9	2	6	6	14
Grand Total				**45**	**12**	**28**	**30**	**70**

X. ASSESSMENT METHODOLOGIES/TOOLS

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Formative assessment (Assessment for Learning)

- Two offline unit tests of 30 marks and average of two unit test.
- For formative assessment of Laboratory learning 25 marks marks will be consider for out of 30 marks
- Each practical will be assessed considering 60% weightage to process, 40% weightage to product.

Summative Assessment (Assessment of Learning)

- End semester assessment of 70 marks.
- End semester summative assessment of 25 marks for laboratory learning

XI. SUGGESTED COS - POS MATRIX FORM

Course Outcomes (COs)	Programme Outcomes (POs)							Programme Specific Outcomes* (PSOs)		
	PO-1 Basic and Discipline Specific Knowledge	PO-2 Problem Analysis	PO-3 Design/ Development of Solutions	PO-4 Engineering Tools	PO-5 Engineering Practices for Society, Sustainability and Environment	PO-6 Project Management	PO-7 Life Long Learning	PSO-1	PSO-2	PSO-3
CO1	2	1	1	1	-	1	1			
CO2	2	1	2	2	-	1	1			
CO3	2	-	-	1	-	-	1			
CO4	2	1	2	2	-	1	1			
CO5	2	1	2	2	-	1	1			

Legends :- High:03, Medium:02,Low:01, No Mapping: -
*PSOs are to be formulated at institute level

XII. SUGGESTED LEARNING MATERIALS / BOOKS

Sr.No	Author	Title	Publisher with ISBN Number
1	Jain R.P.	Modern Digital Electronics	McGraw Hill Education , New Delhi, 2016, ISBN: 978-0070669116
2	Leach Donald P., Malvino Albert Paul, Saha Gautam	Digital Principles and Applications 5/E	Tata McGraw Hill Education, New Delhi, ISBN: 978-0028018218
3	Savaliya M. T.	8086 Programming and advanced processor architecture	Wiley India New Delhi, 2013, ISBN: 978-8126530915
4	Bhurchandi K. M., Roy A. K.	Advanced microprocessors and peripherals 3/E	Tata McGraw Hill Education, New Delhi, 2016, ISBN:9781259006135
5	Triebel, Walter, Singh A., Avtar	The 8088 and 8086 Microprocessors	SCITECH Publications, Chennai 2015, ISBN:978-8183717021

XIII . LEARNING WEBSITES & PORTALS

Sr.No	Link / Portal	Description
1	https://dld-iitb.vlabs.ac.in/	Virtual Lab IIT, Bombay
2	https://www.falstad.com/circuit/	Paul Falstad Circuit Simulator
3	https://logic.ly/	Online Simulator for Digital Techniques

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Sr.No	Link / Portal	Description
4	https://cse15-iiith.vlabs.ac.in/	Virtual Lab IIT, Delhi

Note :

- Teachers are requested to check the creative common license status/financial implications of the suggested online educational resources before use by the students

MSBTE Approval Dt. 02/07/2024 **Semester - 3, K Scheme**